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10/025,760	12/26/2001	John F. Zumkehr	219.40219X00	1662

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EXAMINER	
TABONE JR, JOHN J	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/025,760	Applicant(s) ZUMKEHR, JOHN F.	
	Examiner John J Tabone, Jr.	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 1.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-28 have been examined.

Claim Objections

2. Claim 22 objected to because of the following informalities: This claim is stated as being dependent on claim 23, which is improper. For purpose of examination the Examiner is reading claim 22 as being dependent on claim 21, which follows the same dependencies set up in claims 7 and 8, and 15 and 16. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 20-23 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 20-22:

These claims recite the limitation "said clock generating logic". There is insufficient antecedent basis for this limitation in the claim. The phrase should read instead "said clock generating circuit". Correction is required.

Claim 23:

The claim limitation "adjusting one of a clock" is unclear and ambiguous and, therefore, renders the claim indefinite. Correction and clarification is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 2, 4, 6-10, 12, 14-17, 20-24, and 26-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Sanghani (US-2003/0101376 A1).

Claims 1, 9, and 23:

Sanghani teaches that test patterns produced by LFSR 200 (pattern generating device) are applied to the DDR I/O interface (DDR I/O cell of claim 9; DDR device of claim 23) (e.g., macro cell 100 of FIG. 1A) and then received at the evaluation/result circuitry (pattern checking device) of FIG. 1B, through receive buffer 124 (buffer device), for comparison and error generation. (Page 2, ¶ 31). Sanghani also teaches a single clock is produced on-chip, with PLL 804, for BIST (clock generating circuit). This clock is used to drive the DDR input and output macros as well as the clock macros. (Page 4, ¶ 60).

Claim 17:

"A clock generating circuit to generate a first clock signal and a second clock signal for a DDR device,"

This claim limitation is rejected per claim 1 above.

"wherein said clock generating circuit generates said first clock signal in phase with said second clock signal when in a test mode"

Sanghani teaches during BIST (test mode) transmit and receive clocks may be balanced (in phase) or lock-up latches may be used when a scan chain transitions from a transmit macro to a receive macro (or vice-versa). (Page 4, ¶ 55).

"and generates said first clock signal out of phase with said second clock signal when in a normal mode."

Sanghani teaches in a normal operating mode clock input may be differential (e.g., two 1/2 frequency clocks, one of them being 180 degrees out of phase with the other). (Page 4, ¶ 55).

Claims 2, 10, and 24:

Sanghani teaches during BIST (test mode) transmit and receive clocks may be balanced (in phase) or lock-up latches may be used when a scan chain transitions from a transmit macro to a receive macro (or vice-versa). (Page 4, ¶ 55).

Claims 4, 12, and 26:

Sanghani teaches in a normal operating mode clock input may be differential (e.g., two 1/2 frequency clocks, one of them being 180 degrees out of phase with the other). (Page 4, ¶ 55).

Claims 6, 14, and 20:

Sanghani teaches in the clock output macro 500 (clock generating logic) TxCLK comprises one clock signal for each five bits of data produced by DDR output macro cell 100 (e.g., Tx[4:0]in FIG. 1A) and the two signals are delay matched (through delay elements 514 and 516) for source synchronous operation. (Page 3, ¶ 41; Fig. 5A).

Claims 7, 15, 21, and 27:

Sanghani teaches the multiplexers 102 and 106 (at least one switching element), select between the functional data and BIST signal patterns (a plurality of different modes) depending on the status of bist_en signal 110. (Page 2, ¶ 28).

Claim 28:

This claim is rejected per rejection of claims 6, 14, and 20:

Claims 8, 16, and 22:

Sanghani teaches the status of the bist_en signal 110 controls the state of multiplexers 102 and 106, high for test mode, low for normal mode. (Page 2, ¶ 28). Sanghani also illustrates the bist_en signal 110 being generated from the I/O BIST Controller 802 (state logic to control signals applied to said at least one switching element) in Fig. 8.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3, 11, 18, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sanghani (US-2003/0101376 A1) in view of Fought (US-2003/0005374 A1).

Claims 3, 11, 18, and 25:

Sanghani does not explicitly teach that the test mode comprises an AC I/O loopback test, however, Sanghani does teach the DDR I/O interface provides built-in self-testability (BIST) comprising the test mode. (Page 1, ¶ 5 and 19; page 2, ¶ 20, 25). Fought teaches an AC I/O loopback arrangement using I/O buffer BIST in Fig. 2. (Page 2, ¶ 19, 20, Fig. 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sanghani's BIST circuit to include Fought's AC I/O loopback arrangement. The artisan would be motivated to do so because the improvement on an AC I/O loopback structure using BIST by internally generating the data as compared to loading the data into the flip-flop circuits. This saves a significant amount of testing time. Comparisons can be performed internally within the chip. Accordingly, the external testing device does not need to load the test data into the chip and subsequently perform the comparison. The data may be loaded internally, the comparison may be done internally and the results may be fed out through pins of the chip. Also, the artisan would be motivated to do so because the use of a DDR I/O interface that is self-testable (BIST) eliminates the need for specialized external testing equipment. Such equipment has become increasingly expensive as manufacturers strive to support DDR waveforms and match the operating rates of the interfaces.

6. Claims 5, 13, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sanghani (US-2003/0101376 A1) in view of Corbin (US-6658604).

Claims 5, 13, 19:

Sanghani does not explicitly teach said buffer devices are provided within a memory contoller, however, Sanghani does teach DDR I/O interface that is self-testable. (Page 1, ¶ 19). Corbin teaches of a DDR SDRAM, where the DRAM read cycles have been enhanced to include the addition of a data strobe (DQS). When the data strobe arrives at the memory controller, it is delayed by some amount and then used to latch the data into the memory controller. (Col. 2, lines 1-30). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sanghani's DDR I/O interface to be incorporated into Corbin's DDR SRAM memory controller to align the data strobe with the clock. The artisan would be motivated to do so because this would enable Sanghani's DDR I/O interface to self-test the I/O interface of Corbin's DDR SRAM and produce better edge strobe measurement and eliminates the need for specialized test equipment.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J Tabone, Jr. whose telephone number is (703) 305-8915. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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